UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,464	03/31/2004	Todd B. Myers	884.B60US1	6373

21186 7590 08/01/2006

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
PHAN, THIEM D	
ART UNIT	**PAPER NUMBER**
3729	

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,464	MYERS ET AL.	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-37,39-45 and 69-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-37,39-45 and 69-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 6/05/06 has been fully considered and made of record.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 71 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The claimed language "forming a transformer within the via" (Claim 71, line 2) is neither described nor disclosed in the specification and the drawings. Therefore, that language ""forming a transformer within the via" is a new matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 32-37, 39-45 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crockett et al (US 2002/0100612).

With regard to claims 32 and 39, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board:

- forming a via (Fig. 2, 250B) in a substrate (Fig. 2, 200); and
- forming an electrical component (Fig. 2, 240) in the via in the substrate, wherein the electrical component includes capacitor, resistor, inductor, diode, etc ... (Paragraph 26, line 4); except for designating the later ones as portion of memory.

It would be obvious to one of ordinary skill in the art at the time the invention was made to realize that a memory device such as EEPROM, micropressor or microcontroller has structural layers or circuit layers, which embed large number of capacitors, diodes, inductors or pins in addition to their millions of transistors in order to operate the memory circuit portion without being disturbed by noise, signal interference, etc... Therefore, these electrical components can be considered as part of a memory device.

With regard to claim 33, Crockett et al teach the forming at least of a portion of a resistor (Paragr. 26, line 4).

With regard to claim 34, Crockett et al teach the forming at least of a portion of a capacitor (Paragr. 26, line 4).

With regard to claim 35, Crockett et al teach the forming at least of a portion of a core or inductor or a transformer (Paragr. 26, line 4).

With regard to claim 36, Crockett et al teach the forming of a resistor (Paragr. 26, line 4).

With regard to claim 37, Crockett et al teach the forming of a core or inductor (Paragr. 26, line 4).

With regard to claims 40 and 41, Crockett et al teach the forming of a passive electrical component (Paragr. 26, line 4).

With regard to claims 42-44, Crockett et al teach the forming of an electrical component (Fig. 3A-C, 240; Paragr. 26, line 4) embedded in a via (Fig. 3A-C, 250B).

The limitations of the claims "...a capacitor further comprising: ... an inner cylindrical portion (or a first curved portion) ... an outer via portion (or a second curved portion) ...." are considered to be of a claimed article wherein the process for embedding an electric component in a via operates so this manner of operation does not distinguish over the process of Crockett et al, and Crockett et al at a minimum suggest the claimed method invention.

With regard to claim 45, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board:

- forming a via (Fig. 2, 250B) in a substrate (Fig. 2, 200); and
- forming an electrical component (Fig. 2, 240) in the via in the substrate, wherein the electrical component includes capacitor, resistor, inductor, diode, etc ... (Paragraph 26, line 4); except for designating the later ones as portion of a transformer.

It would be obvious to one of ordinary skill in the art at the time the invention was made to realize that some transformers have structural layers or circuit layers, which embed many capacitors, diodes, inductors or pins in addition to their windings and cores in order to operate the transformer portion without being disturbed by noise, signal interference, etc... Therefore,

these electrical components can be considered as part of a transformer.

With regard to claim 71, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board, including the forming of a via (Fig. 2, 250B) in a substrate (Fig. 2, 200) and the forming of an electrical component (Fig. 2, 240) in the via in the substrate, wherein the electrical component includes capacitor, resistor, inductor, diode, etc ... (Paragraph 26, line 4); except for designating the later ones as a transformer.

It would be obvious to one of ordinary skill in the art at the time the invention was made to realize that a transformer can be purely made of diodes to form step-up or step-down or converter transformers or the like. Therefore, these electrical components can be built into a transformer.

6. Claims 42-44, 69 and 70 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Crockett et al in view of Figueroa et al (US 6,446,317).

With regard to claim 42, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board including the embedding of capacitor (Fig. 3A-C, 240) in the via (Fig. 3B, 250B), which reads on applicants' claimed invention; except for describing a capacitor configuration, which is well known in the art.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- an inner cylindrical portion (Fig. 4, 406); and

- an outer via portion (Fig. 4, 404) substantially surrounding the inner cylindrical portion.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the detailed description of the capacitor, as taught by Figueroa et al, to the method of embedding the capacitor in the via of Crockett et al in order to have a clearer picture of a capacitor.

With regard to claim 43, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board including the embedding of capacitor of curvature shape (Fig. 3B, 240) in the via (Fig. 3B, 250B), which reads on applicants' claimed invention; except for describing a curved capacitor configuration, which is well known in the art.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- a first curved portion (Fig. 4, 406); and
- a second curved portion (Fig. 4, 404) spaced from the first curved portion by a dielectric (Fig. 4, 408).

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the detailed description of the capacitor, as taught by Figueroa et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to have curved portions of the curved capacitor with varying dielectric thickness.

As applied to claim 44, Crockett et al teach a method for reducing the impedance within

the reference within the printed circuit board including the embedding of capacitor of curvature shape (Fig. 3B, 240) in the via (Fig. 3B, 250B), which reads on applicants' claimed invention; except for describing a curved capacitor configuration, which is well known in the art.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- a first curved portion (Fig. 4, 406); and
- a second curved portion (Fig. 4, 404) spaced from the first portion by a dielectric (Fig. 4, 408),

  wherein the first portion and the second portion are portions of a via formed by insulating (Fig. 4, 408) a first curved portion of the via from a second curved portion of the via.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the detailed description of the capacitor, as taught by Figueroa et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to have curved portions of the curved capacitor with insulating dielectric.

With regard to claim 69, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board, including the forming of a via (Fig. 2, 250B) in a substrate (Fig. 2, 200), the forming of a capacitor (Fig. 2, 240) in the via in the substrate and the embedding of a capacitor of curvature shape (Fig. 3B, 240) in the via, which read on applicants' claimed invention.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- forming a first curved portion (Fig. 4, 406); and
- forming a second curved portion (Fig. 4, 404) spaced from the first curved portion by a dielectric (Fig. 4, 408), in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the method of fabricating the hybrid capacitor, as taught by Figueroa et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge in a crowded circuitry.

With regard to claim 70, Crockett et al teach a method for reducing the impedance within the reference within the printed circuit board, including the forming of a via (Fig. 2, 250B) in a substrate (Fig. 2, 200), the forming of a capacitor (Fig. 2, 240) in the via in the substrate and the embedding of a capacitor of curvature shape (Fig. 3B, 240) in the via, which read on applicants' claimed invention.

Figueroa et al teach a method of fabricating a hybrid capacitor embedded in a via, comprising:

- forming a first curved portion (Fig. 4, 406); and
- forming a second curved portion (Fig. 4, 404) spaced from the first curved portion by a

dielectric (Fig. 4, 408), wherein the first portion and the second portion are portions of a via formed by insulating (Fig. 4, 408) a first portion of the via from a second portion of the via, in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the method of fabricating the hybrid capacitor, as taught by Figueroa et al, to the method of embedding the curved capacitor in the via of Crockett et al in order to increase levels of capacitance at reduced levels of inductance for decoupling, power dampening and supplying charge in a crowded circuitry.

Response to Arguments

7. Applicants' arguments with respect to claims 32-45 and 69-71 have been considered but are moot in view of the new and current grounds of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Applicants' amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim Phan
Examiner
Art Unit 3729

A. DEXTER TUGBANG
PRIMARY EXAMINER

tp
July 26, 2006

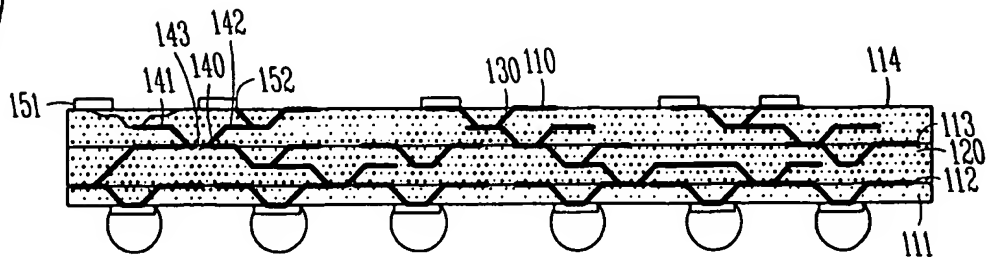

FIG. 1

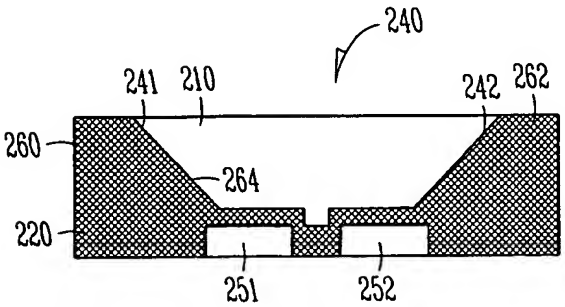

FIG. 2

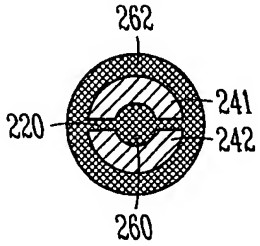

FIG. 3

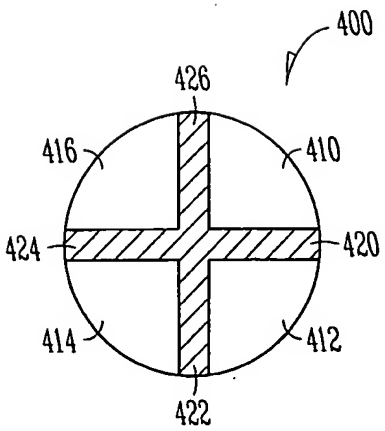

FIG. 4

OK to enter!
TDP 7/26/06